

Electrical and Structural Characterization of Web Dendrite Crystals

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Abstract

Minority carrier lifetime distributions in silicon web dendrites are measured. Emphasis is placed on measuring areal homogeneity of lifetime, show its dependency on structural defects, and its unique change during hot processing. The internal gettering action of defect layers present in web crystals and their relation to minority carrier lifetime distributions is discussed. Minority carrier lifetime maps of web dendrites obtained before and after high temperature heat treatment are compared to similar maps obtained from 100 mm diameter Czochralski silicon wafers. Such maps indicate similar or superior areal homogeneity of minority carrier lifetime in webs.

Introduction

Recently, calculations have been made which show that the presence of areal inhomogeneity of minority carrier lifetime in silicon wafers can devastate solar cell efficiency (1). For instance, it was shown that for no more than 5% of the solar cell area being inferior compared to the rest of the cell area, solar cell efficiency can be as poor as it would be if the entire area would be of inferior quality (1). Thus areal homogeneity of minority carrier lifetime is an important requirement for high efficiency solar cells.

This paper reports measurements of minority carrier lifetime "distributions" made on silicon web dendrite sections. Such measurements are compared to similar data obtained from 100 mm diameter Czochralski silicon wafers.

Structural Aspects of Silicon Web

A brief description of the as-grown web geometry and dislocation structure is needed to describe our electrical measurements clearly. For detailed results we refer to the original papers on web growth (2) and dislocation structures (3-5).

The web surface is parallel to the (111) plane, and the web pulling direction is $[2\bar{1}\bar{1}]$. A cross-section of web shows its most prominent structural feature: multiple twin lamellae in the center of the web covered by two thick (100 μm) surface layers which are also in twin relation. An example is shown in Figs. 1a,b.

Dislocations in web are generated through "melt entrapment" caused by "wing" growth along the dendrites (Fig. 2). Propagation of such dislocations depends on the curvature of the solid-liquid interface of the web during growth. An interface curvature of concave downward concentrates the dislocations in the center of the web (Fig. 3). Webs grown with a straight interface concentrate the dislocations in the fillet region. Thus the web grows free of any dislocations (4), Fig. 4. Most webs of today contain bundles of very long dislocation lines parallel to the $[2\bar{1}1]$ direction (Fig. 5). They are piled up against the twin planes. In addition, annealed web contains large area stacking faults. The electrical activity and the influence of these faults on solar cell efficiency has not yet been investigated. Such an influence is assumed to be relatively small but it may be of importance for high efficiency solar cells. These defects are described in more detail in References 3 and 5, examples are shown in the x-ray topographs of Figs. 6.

If excessive stresses are present during web growth (buckling) large numbers of slip dislocations and small angle grain boundaries may occur. Such defects degrade minority carrier lifetime. An example is shown in the x-ray topographs of Figs. 7.

Minority Carrier Lifetime Measurement In Web

Silicon web dendrite sections of various quality (Figs. 5, 6, 7) were evaluated through minority carrier lifetime "mapping" using 1.5 mm diameter MOS capacitors. The total number of MOS capacitors per web section was 300. The MOS dots were arranged into 15 rows. The dendrites were included into the evaluation. The dimensions of the web sections were 2 inches long and 32 mm wide. The webs were evaluated after each oxidation cycle (15 min wet-110 min dry-15 min wet at 1000°C. Three or four consecutive oxidation cycles were used. Minority carrier lifetime maps of the total web section were obtained after each oxidation cycle by measuring the lifetime under each capacitor as described by Fahrner & Schneider (6). Subsequently, the lifetime was computer plotted versus its position on the web surface. Local lifetime degrading defects revealed by such lifetime maps were analysed by advanced characterization techniques. A result typical for web sections of quality as shown in Figs. 5 and 6 is given in Fig. 8. This figure summarizes the influence of high temperature heat cycles on minority carrier lifetime. The lifetime data are displayed in 6 maps. Each map represents a matrix of 300 capacitor dots. The maps on the left side of the figure carry the label oxidation 1 to 3 and represent the lifetime data obtained after the first, second, and third oxidation cycle. The devices were obviously stripped before every successive oxidation step. The z-scale represents the measured lifetime values in microseconds. The range of lifetime data present on the web section is also included in the label. For instance, the minimum lifetime obtained at a specific location (capacitor) after the first oxidation was 0.274 microseconds. The maximum lifetime is 207 microseconds. The lifetime map shows a relatively smooth plateau. Noteworthy is, that this plateau extends over the total web section surveyed. Accordingly, this web is of excellent crystal quality and compares well with the best Czochralski silicon as available today. Interesting is a comparison of the maps obtained after the first, second and third oxidation. The lifetime plateau obtained after the second oxidation is well above the one obtained after the first oxidation and the same is true for the third oxidation. The third plateau is a little bit lower than the second one. Using Czochralski wafer quality as a standard, the

material obtained after the third oxidation shows very uniform lifetime distribution data.

The maps on the right side of Fig. 8 are labeled DECREASE or INCREASE. The DECREASE map shows the degradation of lifetime as a result of the second or third oxidation cycle. The INCREASE map shows the area where the lifetime increased after the third oxidation relative to the first oxidation. These maps show clearly the improvement of lifetime as a result of oxidation. This improvement is fairly uniform and covers practically the total web area. Decreases in lifetime occur only along the dendrites, the fillet region or along the edges where the web section was cut by the dicing saw. This result is unique and relates to the special crystal structure of the "perfect" web. The defect planes, sandwiched between the perfect web surface layers, provide for "internal" gettering during high temperature heat cycles. Thus a substantial improvement of minority carrier lifetime can result.

Web material of the quality as displayed in the topographs of Figs. 7 do not give comparable results. It was found that the "slip" dislocations - which result from buckling stresses - degrade minority carries lifetime substantially. These dislocations are of the same type as the "process" induced slip dislocation encountered during IC processing. It is known that the electrical activity of these dislocations is high. The lifetime map shown in Fig. 9 corresponds to the sample shown in Fig. 7b. Note the good correlation between low lifetime and defect area in the center of this sample.

Minority Carrier Lifetime Measurements in Czochralski Silicon

Recently, we conducted an evaluation of 100 mm diameter Czochralski silicon wafers as available from major vendors throughout the world. The evaluation concentrated on minority carrier lifetime mapping as described for the web crystal. Four consecutive oxidation cycles were used. The MOS dot matrix consisted of 25 times 25 MOS capacitors of 1.5 mm diameter. A result typical for the evaluated Czochralski wafers is shown in Fig. 10. The lifetime data shown in Fig. 10 are displayed in 4 maps. The maps on the left carry again the oxidation number. The data obtained after the first oxidation indicate excellent wafer quality. The map has a plateau at approx. 250 to 300 microseconds and extends practically across the total wafer area. This wafer represents silicon of the best quality. Nevertheless, successive oxidation results in steady degradation of lifetime. This is seen by comparing the maps obtained after the first and fourth oxidation.

Interesting are the DECREASE and INCREASE maps shown on the right of Fig. 10. The decrease map confirms that degradation occurs uniformly across the total wafer area. After the fourth oxidation cycle small lifetime increases are observed only at 9 locations. In all other areas lifetime degraded substantially.

Discussion and Summary

The data given in Figs. 8 and 10 are representative of "perfect" web and Czochralski silicon wafers. We note a basic difference between these two materials. Oxidation increases generation lifetime in Web but decreases the

same lifetime in Czochralski material. The decrease in lifetime in Czochralski wafers correlates with the precipitation phenomena of oxygen in silicon (7).

The large extent to which areal inhomogeneities exist in today's silicon and influence device performance (1) is not well known. However, uniform minority carrier lifetime distributions are a pre-requisite to high performance solar cell technology. Solar cell efficiency in excess of 15% for large area single crystal silicon cells (10 cm x 10 cm) will be very difficult to achieve without proper control of minority carrier lifetime distributions during large scale manufacturing.

References

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4. T. N. Tucker and G. H. Schwuttke, Appl. Phys. Letter, 9, 219, (1966).
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6. W. Fahrner and C. P. Schneider, J. Electrochem. Soc., 123, 100, (1976).
7. G. H. Schwuttke, Semiconductor Industry Association (SIA) Lecture, Stanford Univ., Sept. 1981, Palo Alto, CA.

Figure Captions

- Fig. 1 a. Web Crystal Geometry
b. SEM-micrograph of cleaved web cross-section after preferential etching. Note twin lamellae in center.
- Fig. 2 SOT X-ray topograph of 2 cm wide web dendrite. Note wing growth (arrows) at dendrites below web leading to liquid entrapment and dislocation generation during growth.
- Fig. 3 SOT X-ray topograph of 3 cm wide web dendrite. Note dislocation generation at stress centers and propagation of dislocations during growth toward center.
- Fig. 4 SOT X-ray topograph of perfect 1.5 cm wide web. Dislocations are trapped in fillet region.
- Fig. 5 SOT X-ray topograph of high performance web 220-reflection. Note long dislocations, 73 degree type; Burgers vectors [101], [110]. Low electrical activity.
- Fig. 6 SOT X-ray topographs of high performance web. Width 3.2 cm.
a. (111) reflection: Surface twin lamellae
b. (111) reflection: Bottom twin lamellae
Note difference in crystal perfection: Bottom lamellae contains large area stacking faults. Topographs recorded after third oxidation. Electrical activity of defects low. Electrical data in Fig. 8.
- Fig. 7 a. SOT X-ray topograph of low quality web. Note slip dislocations. Electrical activity high. Lifetime range: 0.01 - 1 μ sec.
b. SOT X-ray topograph of medium quality web. Electrical data in Fig. 9.
- Fig. 8 Minority carrier lifetime maps of high performance web. Lifetime range: 0.2 - 207 μ sec.
- Fig. 9 Minority carrier lifetime map of low performance web. Corresponding SOT topograph is shown in Fig. 7b. Note correlation between dislocation density and low lifetime. Lifetime range: 0.1 - 50 μ sec.
- Fig. 10 Minority carrier lifetime map of Czochralski wafer for comparison. Lifetime range: 4 - 478 μ sec.

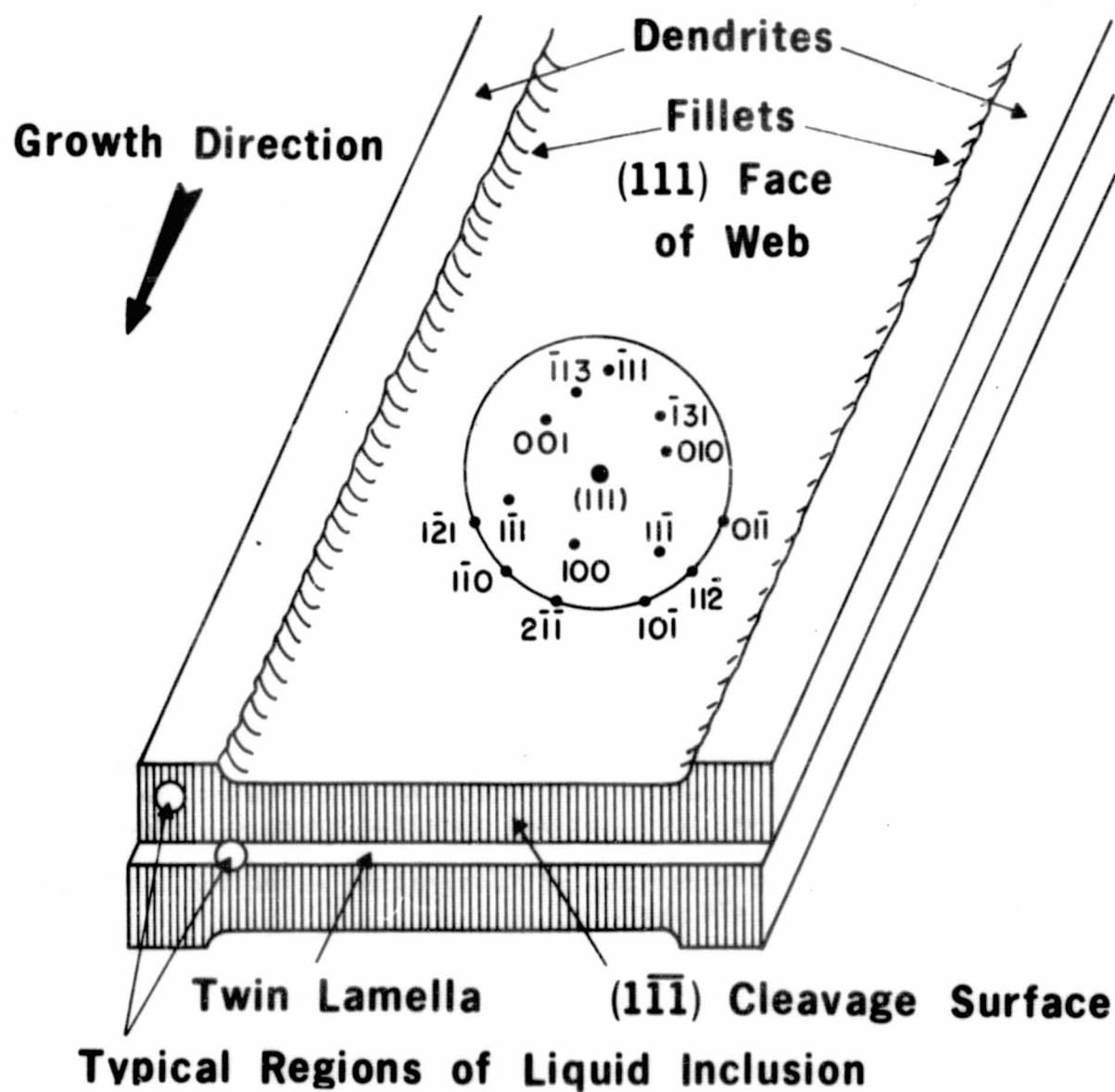


Fig. 1a Web Crystal Geometry

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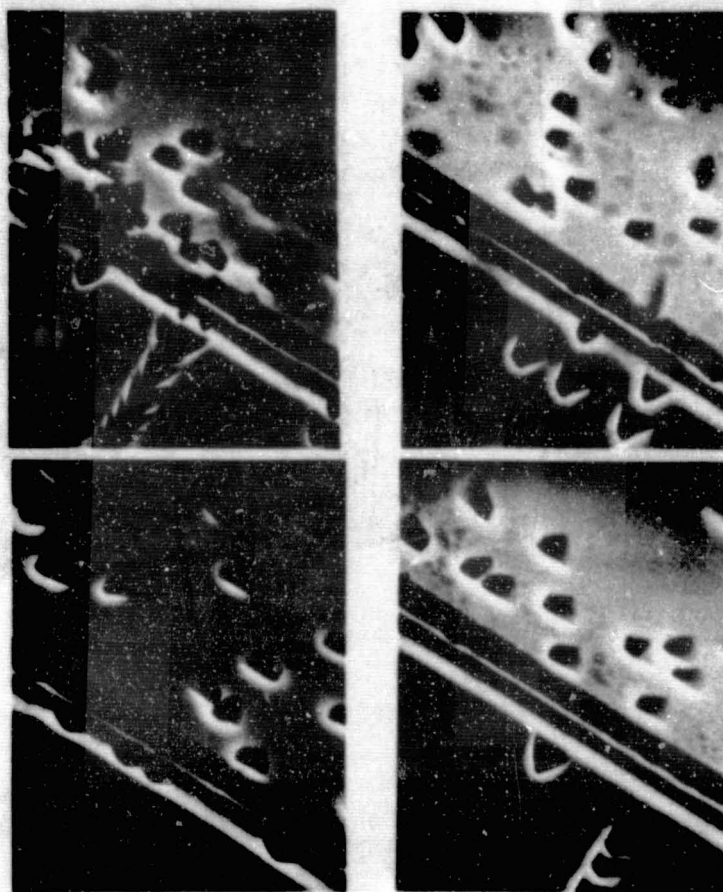


Fig. 1b SEM-micrograph of cleaved web cross-section after preferential etching. Note twin lamellae in center.

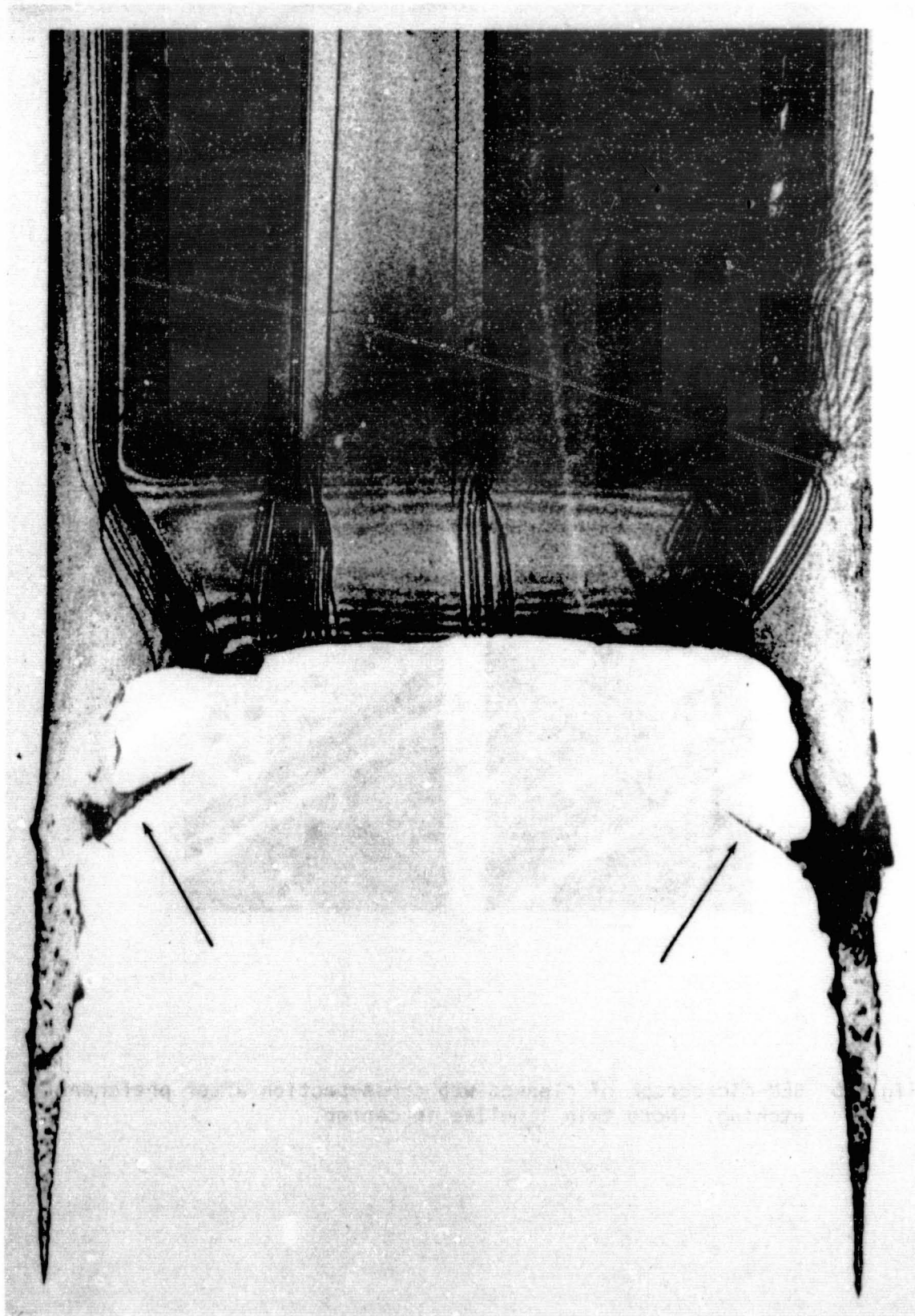


Fig. 2 SOT X-ray topograph of 2 cm wide web dendrite. Note wing growth (arrows) at dendrites below web leading to liquid entrapment and dislocation generation during growth.

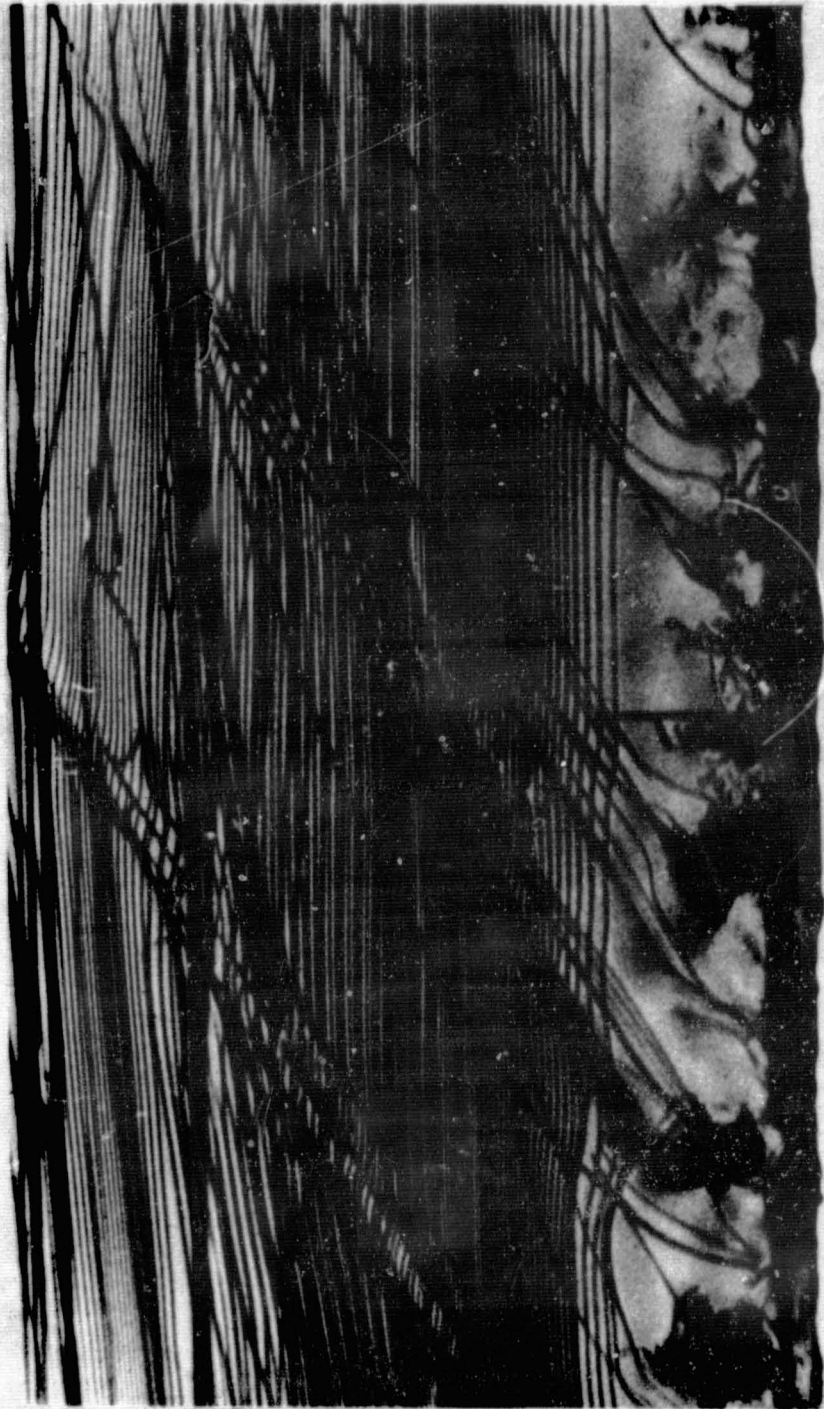


Fig. 3 SOT X-ray topograph of 3 cm wide web dendrite. Note dislocation generation at stress centers and propagation of dislocations during growth toward center.

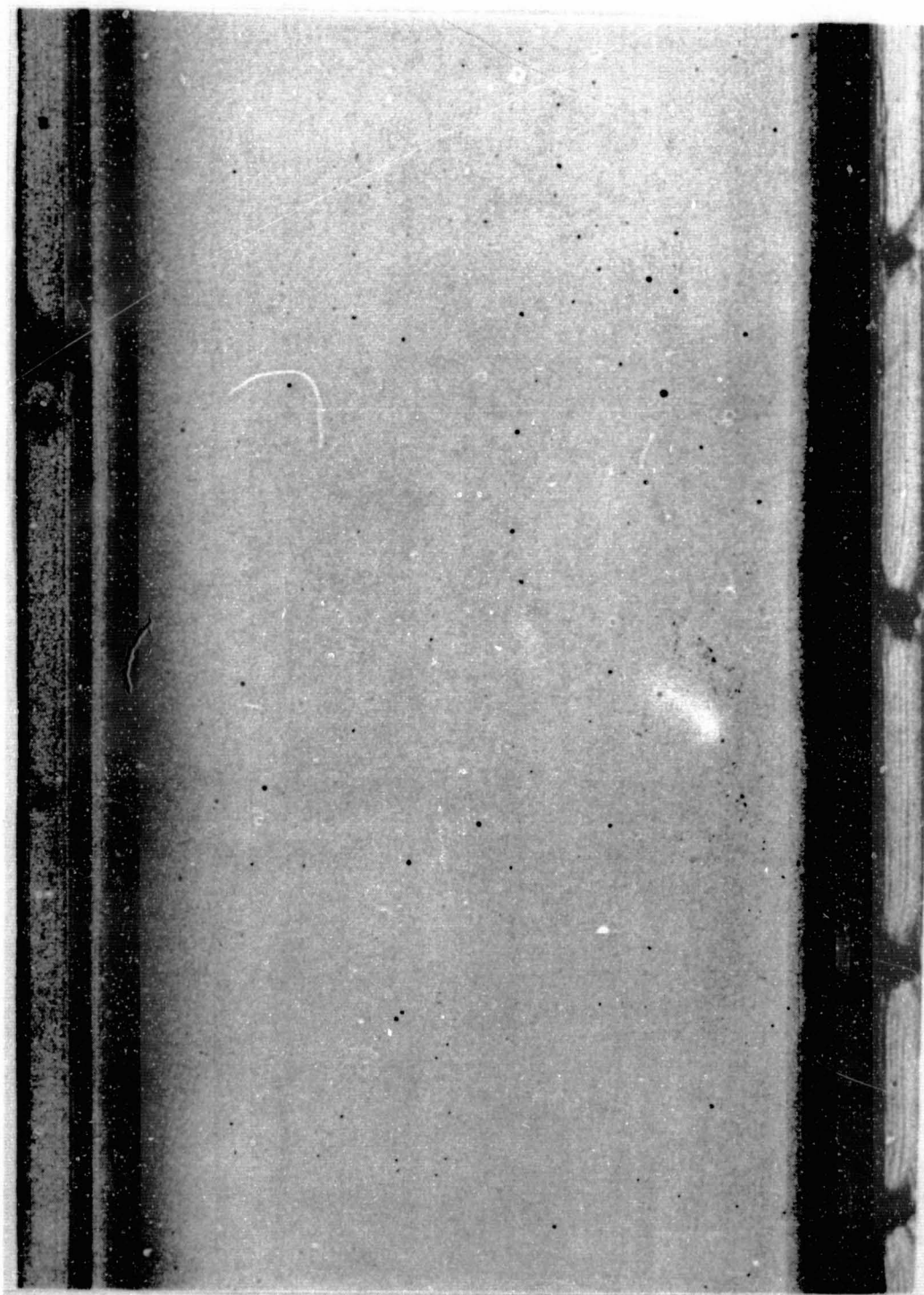


Fig. 4 SOT X-ray topograph of perfect 1.5 cm wide web. Dislocations are trapped in fillet region.

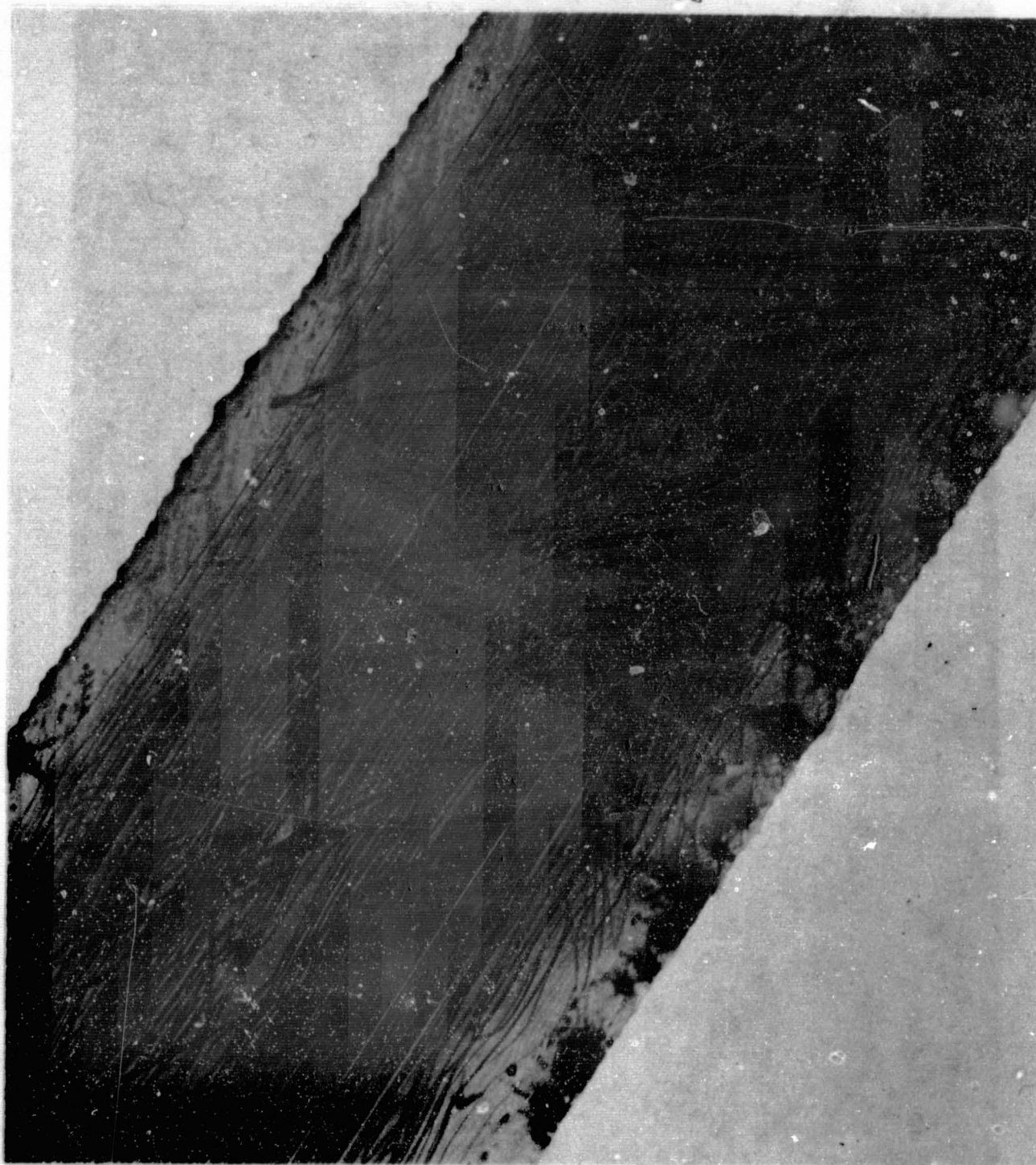


Fig. 5 SOT X-ray topograph of high performance web, 220-reflection. Note long dislocations, 73 degree type; Burgers vectors $[101]$, $[110]$. Low electrical activity.

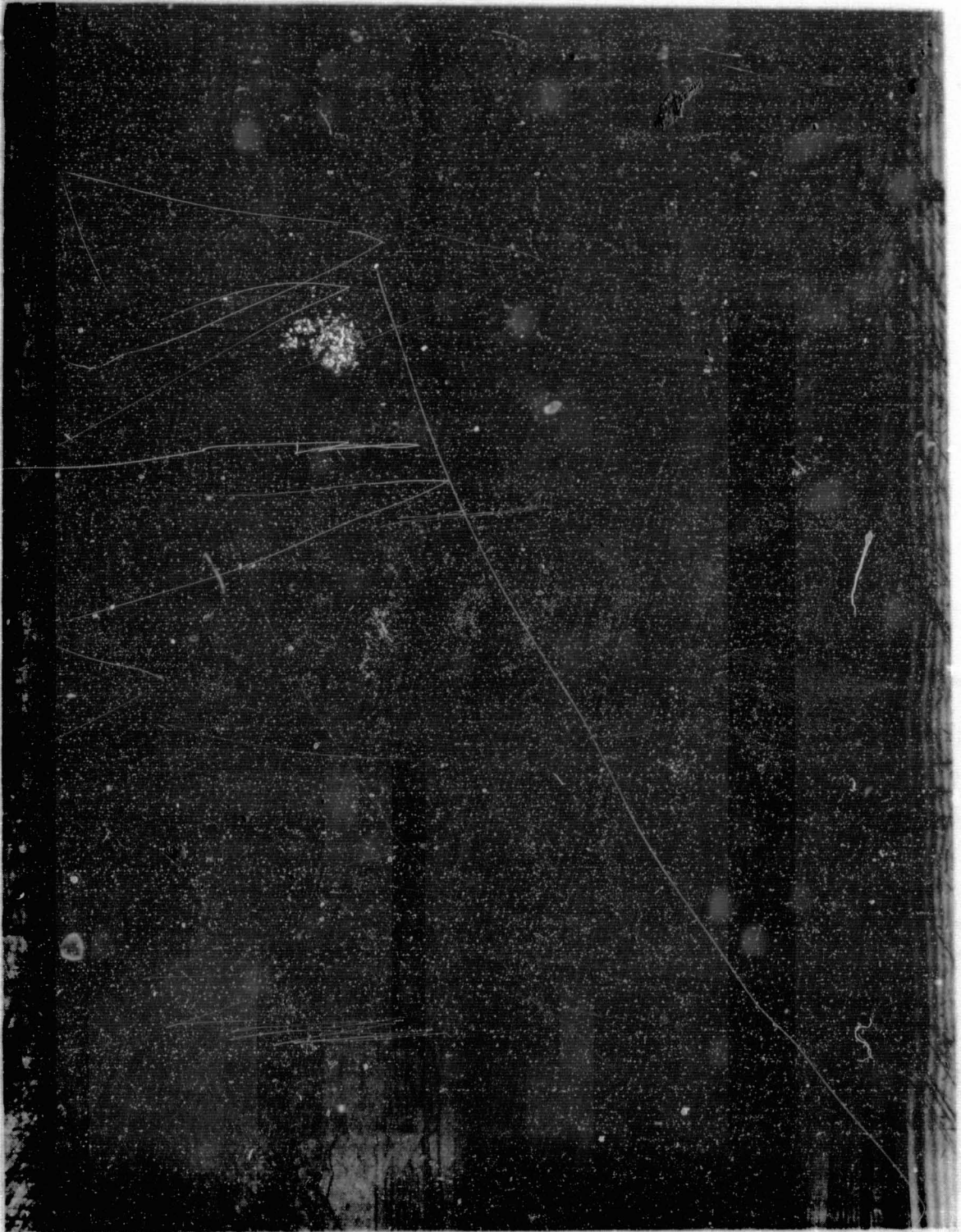


Fig. 6a SOT X-ray topographs of high performance web. Width 3.2 cm.
(111) reflection: Surface twin lamellae.
Electrical data in Fig. 8.



Fig. 6b SOT X-ray topographs of high performance web. Width 3.2 cm.
(111) reflection: Bottom twin lamellae
Note difference in crystal perfection: Bottom lamellae contains
large area stacking faults. Topographs recorded after third
oxidation. Electrical activity of defects low.

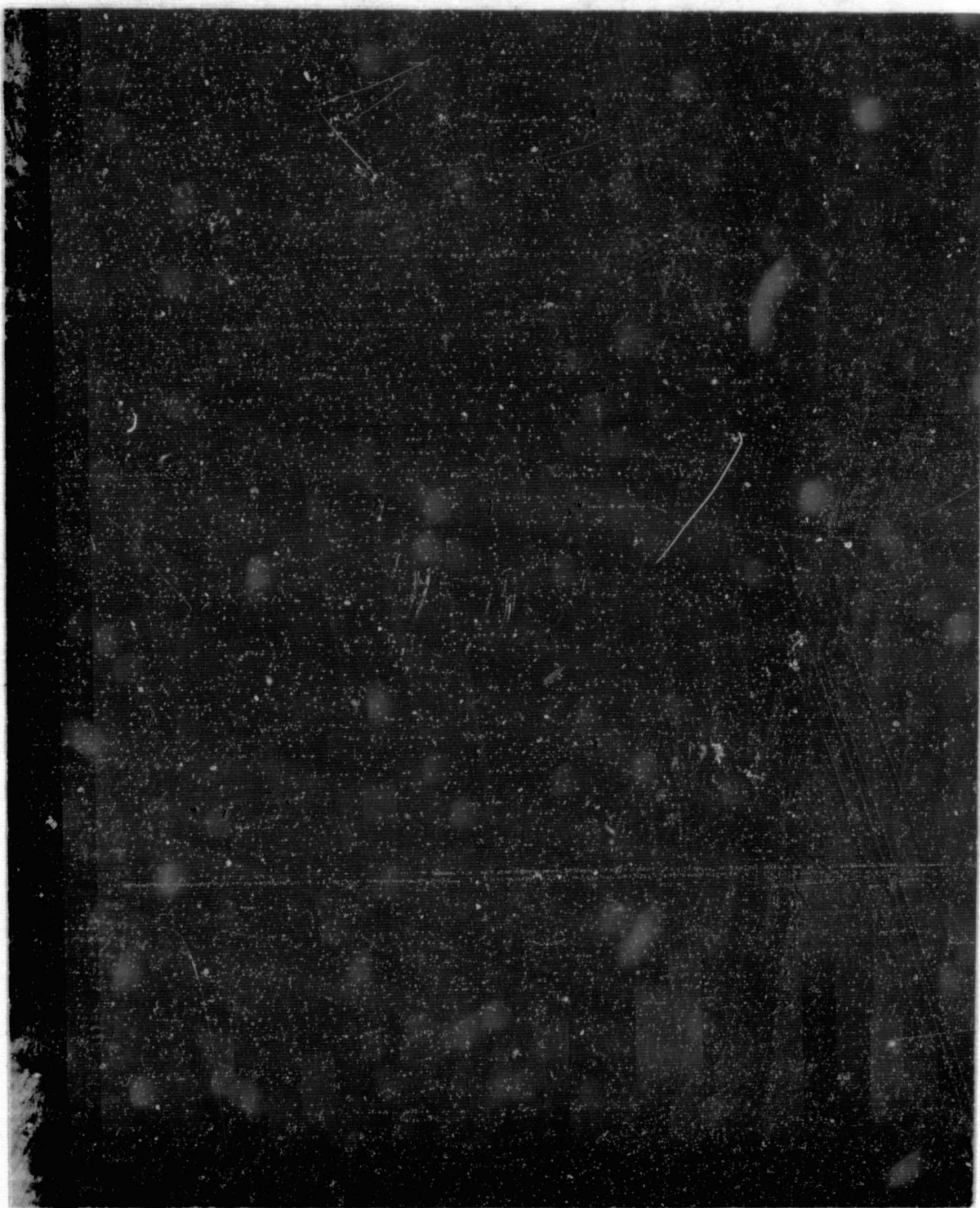


Fig 7a SOT X-ray topograph of low quality web. Note slip dislocations.
Electrical activity high. Lifetime range: 0.01 - 1 μ sec.



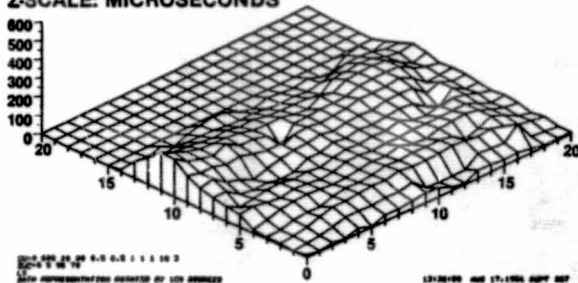
Fig 7b SOT X-ray topograph of medium quality web. Electrical data in Fig. 9.

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Web Dendrite Silicon Lifetime Distribution Data

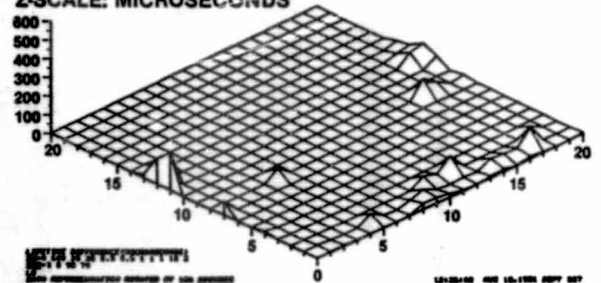
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DATA RANGE: .2740 207
Z-SCALE: MICROSECONDS



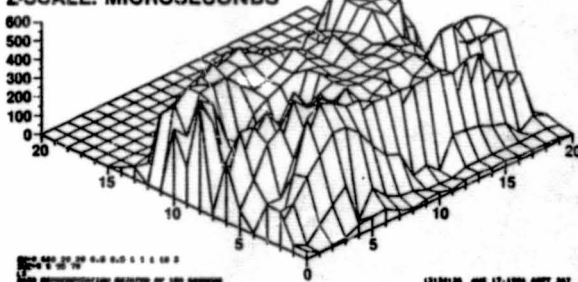
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DATA RANGE: .5000 200
Z-SCALE: MICROSECONDS



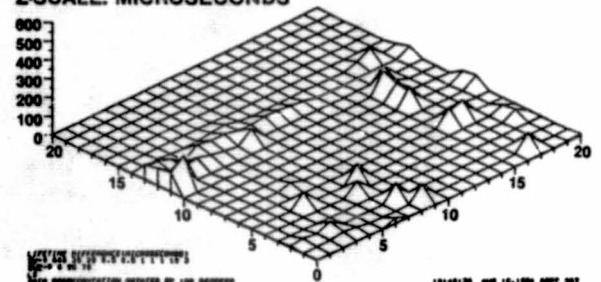
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Z-SCALE: MICROSECONDS



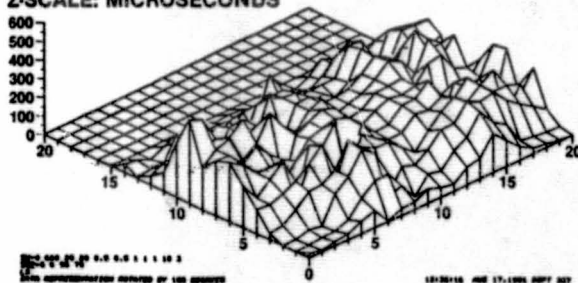
Decrease 1 to 3

OXIDATION NUMBERS: 1 3
DATA RANGE: .1000 163
Z-SCALE: MICROSECONDS



Oxidation 3

NO. OF OXIDATIONS: 3
DATA RANGE: .1810 452
Z-SCALE: MICROSECONDS



Increase 1 to 3

OXIDATION NUMBERS: 1 3
DATA RANGE: .1810 305
Z-SCALE: MICROSECONDS

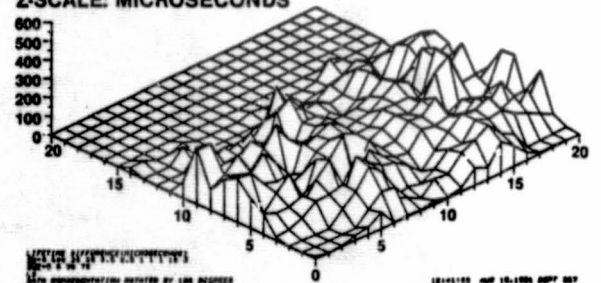
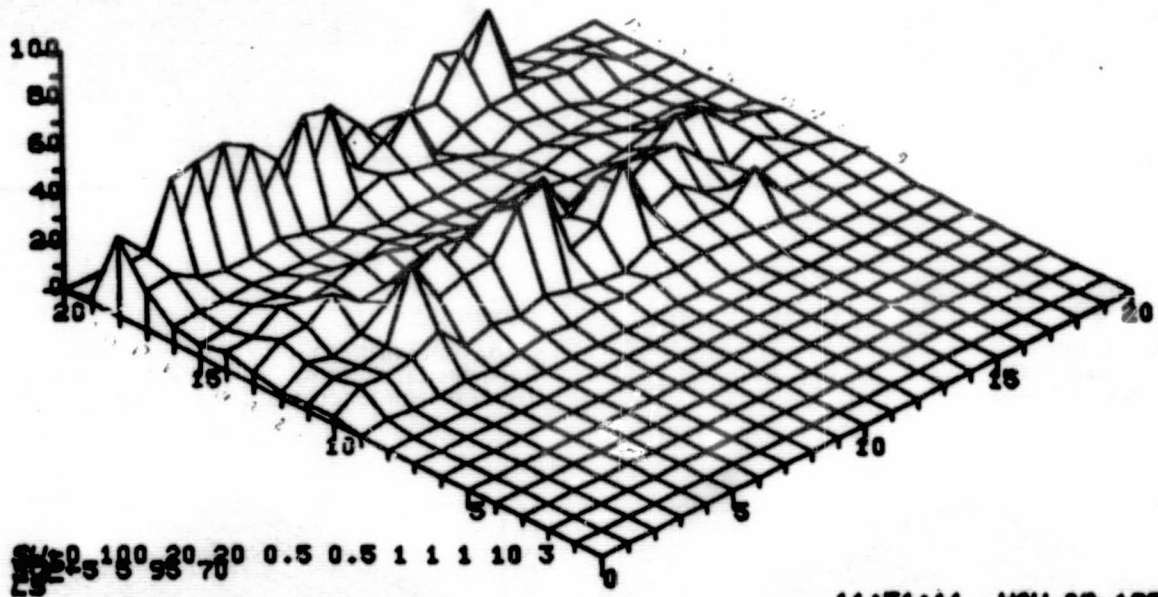


Fig. 8 Minority carrier lifetime maps of high performance web.
Lifetime range: 0.2 - 207 μ sec.

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LIFETIME DATA DISTRIBUTION MAP

WAFER ID: 459
VENDOR:
FILE RECORD: GA135 LIFE1
NO. OF OXIDATIONS: 1
THICKNESS (A): 4800
DATA RANGE: .1160 50
Z-SCALE : MICROSECONDS



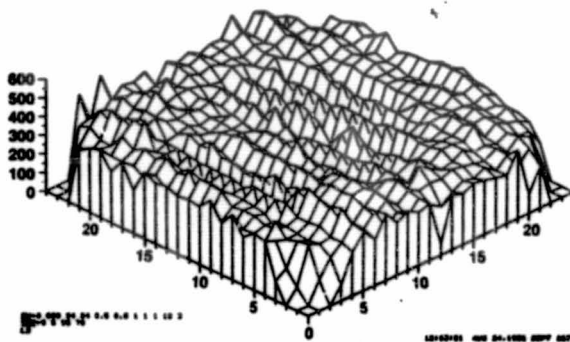
11:51:11 NOV 09, 198

Fig. 9 Minority carrier lifetime map of low performance web. Corresponding SOT topograph is shown in Fig. 7b. Note correlation between dislocation density and low lifetime. Lifetime range: 0.1 - 50 μ sec.

Lifetime Data Distribution Map Vendor B

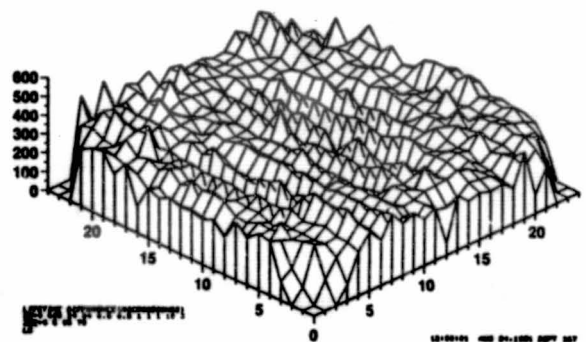
Oxidation 1

NO. OF OXIDATIONS: 1
DATA RANGE: 4.0000 478
Z-SCALE: MICROSECONDS



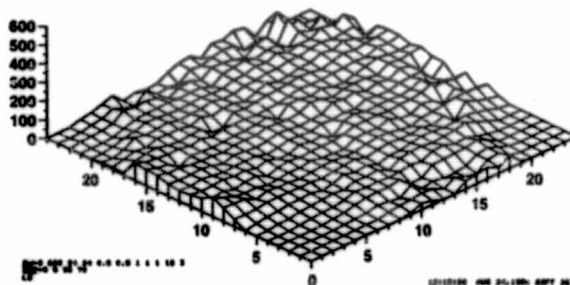
Decrease

OXIDATION NUMBERS: 1 4
DATA RANGE: 7.0000 442
Z-SCALE: MICROSECONDS



Oxidation 4

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DATA RANGE: .5300 129
Z-SCALE: MICROSECONDS



Increase

OXIDATION NUMBERS: 1 4
DATA RANGE: 2.0000 48
Z-SCALE: MICROSECONDS

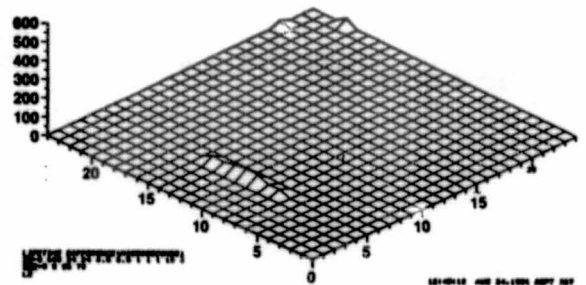


Fig. 10 Minority carrier lifetime map of Czochralski wafer for comparison.
Lifetime range: 478 μ sec.

DISCUSSION

HANOKA: Do you have any idea why the grown dislocations seem to be not electrically bothersome, whereas the stress-induced ones are?

SCHWUTKE: First of all, the core structure of this grown dislocation is very benign. It makes an angle of 73° , and this type of dislocation has been described in the literature. This structure is very benign, while a 60° dislocation, which is a slip dislocation, is very active due to its core structure.